**ECE 429 Lab 8**

**Carry-Ripple Addition III**

**David Cho**

**A20384999**

**04/02/2020**

**Introduction**

The objective of this lab is to use the designs from labs 6 and 7 to create a 4-bit adder. The design functionalities will be verified using LVS and ESP.

**Theory/Pre-Lab**

In order to create a 4-bit carry ripple adder, the adders that were previously designed will be utilized in sequence. Prior to the lab, the following additions were required to be calculated.

1. 11 + 5 = 16

1011 + 0101 = 10000

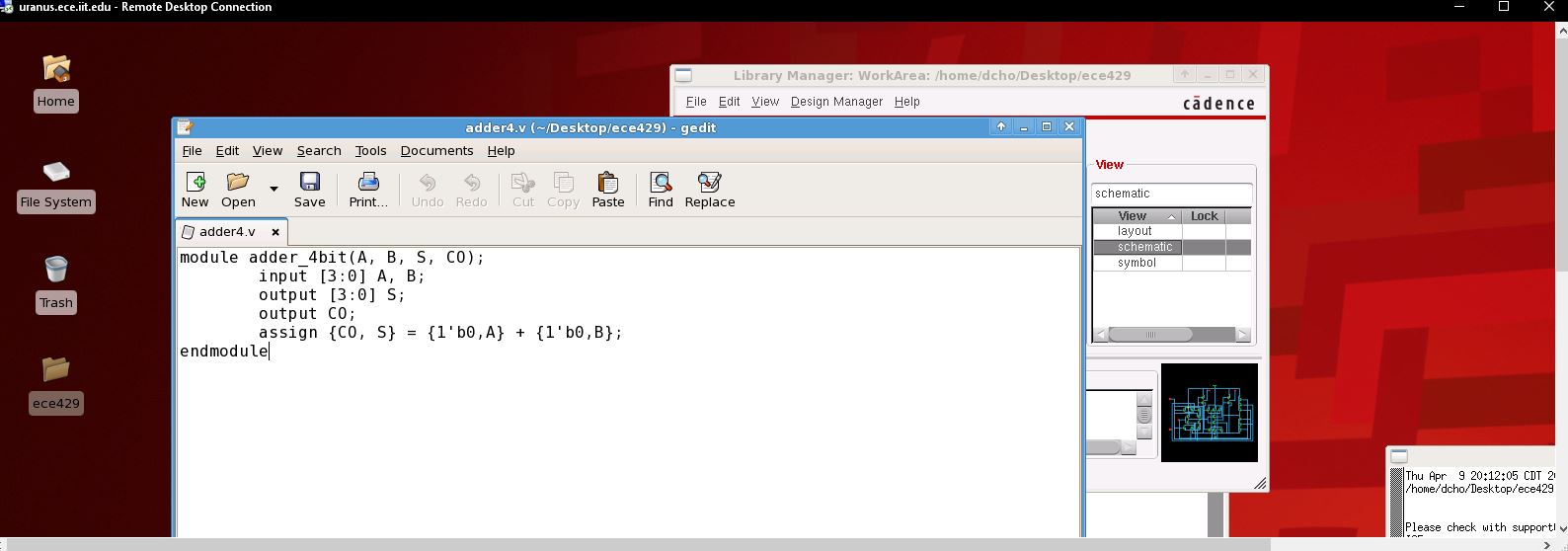
1. 4 + 10 = 14

0100 + 1010 = 1110

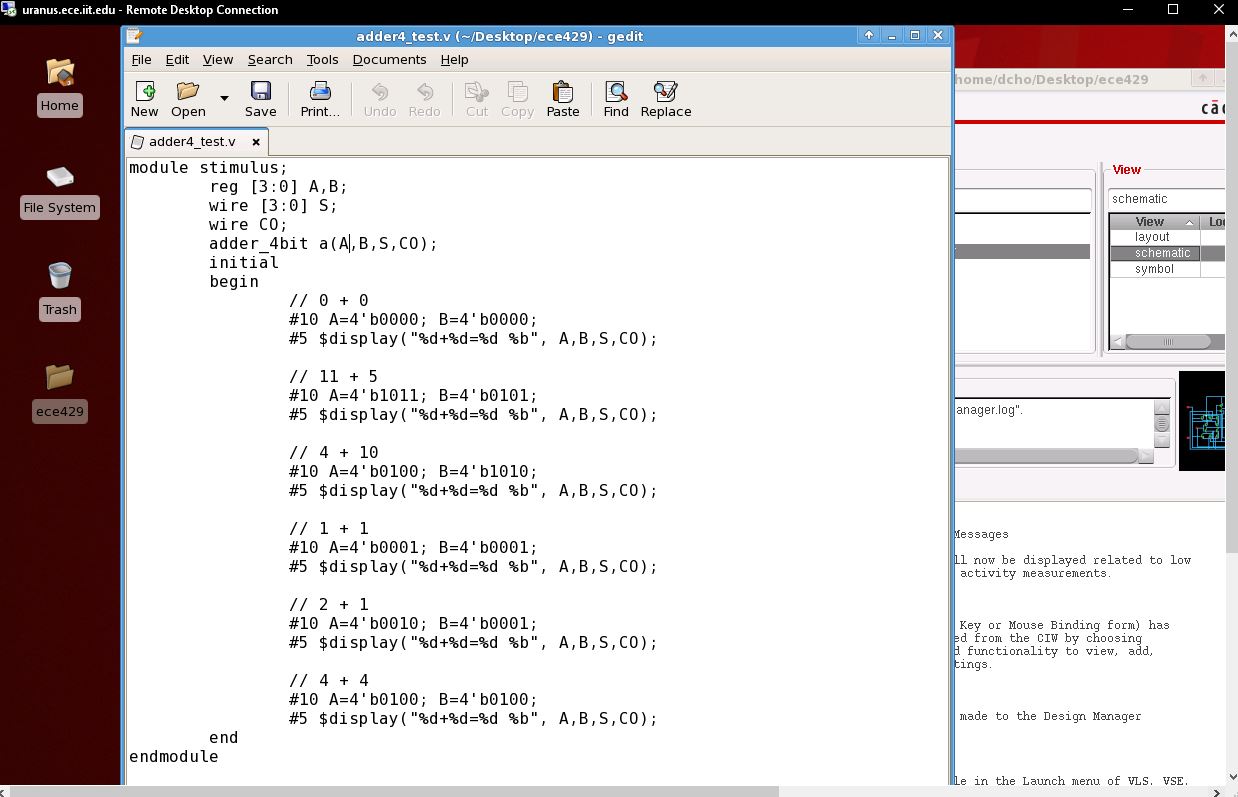
**Implementation**

Using the lab manual, the Verilog files that were used to test the 4-bit adder were created.

**Figure 1: 4-bit Adder Verilog**

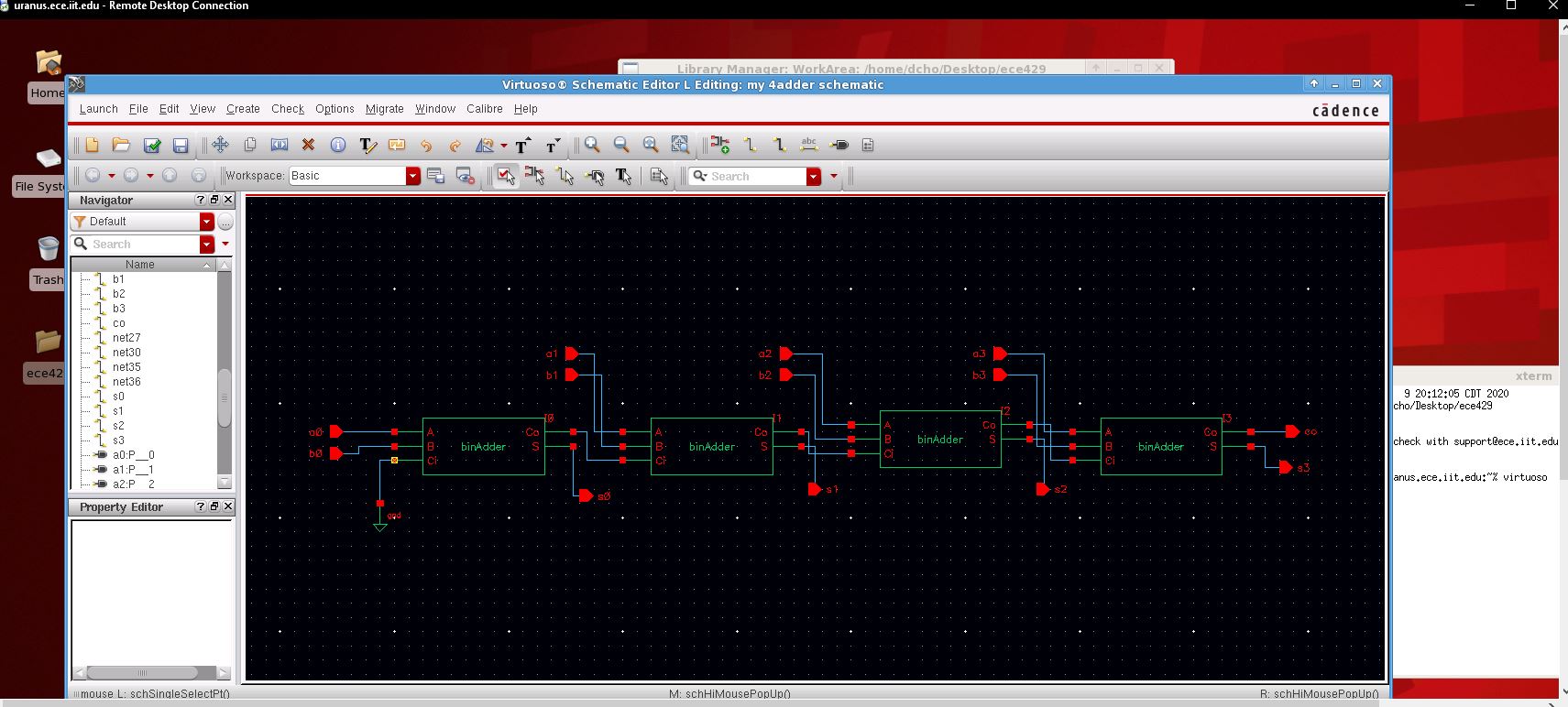
****

**Figure 2: 4-bit Adder Test Verilog**

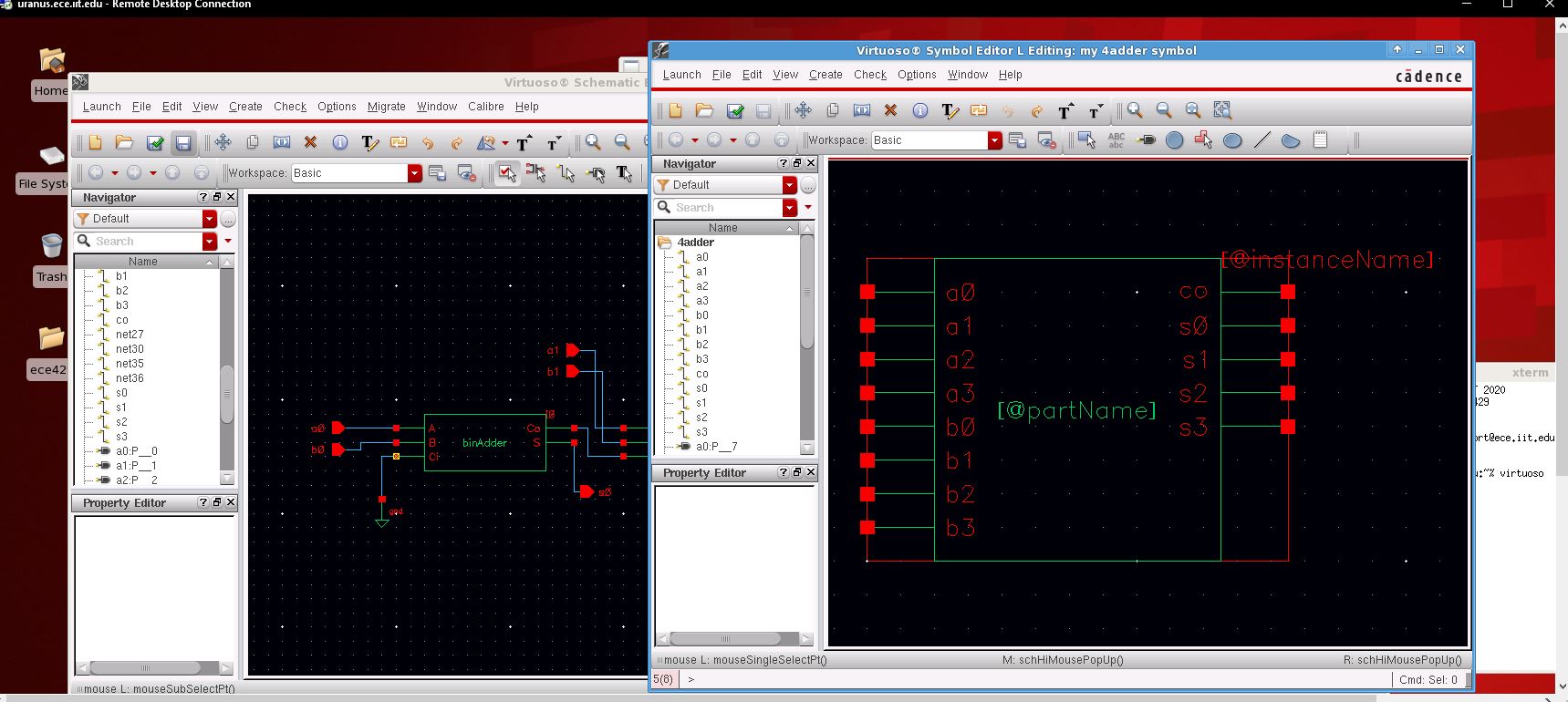
****

Then the video tutorial was followed to create the schematic, symbol, and layout. The layout was tested using DRC and LVS.

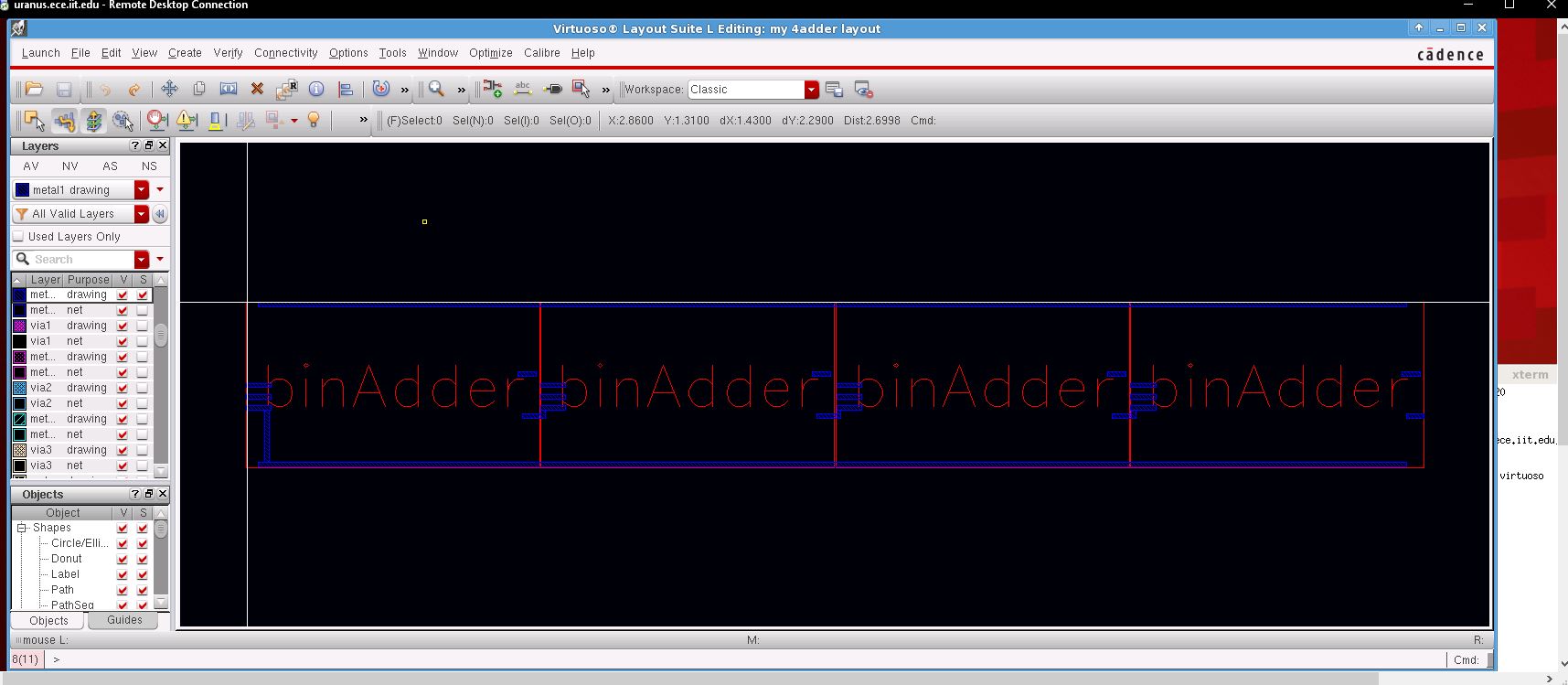
**Figure 3: 4-bit Adder Schematic**

****

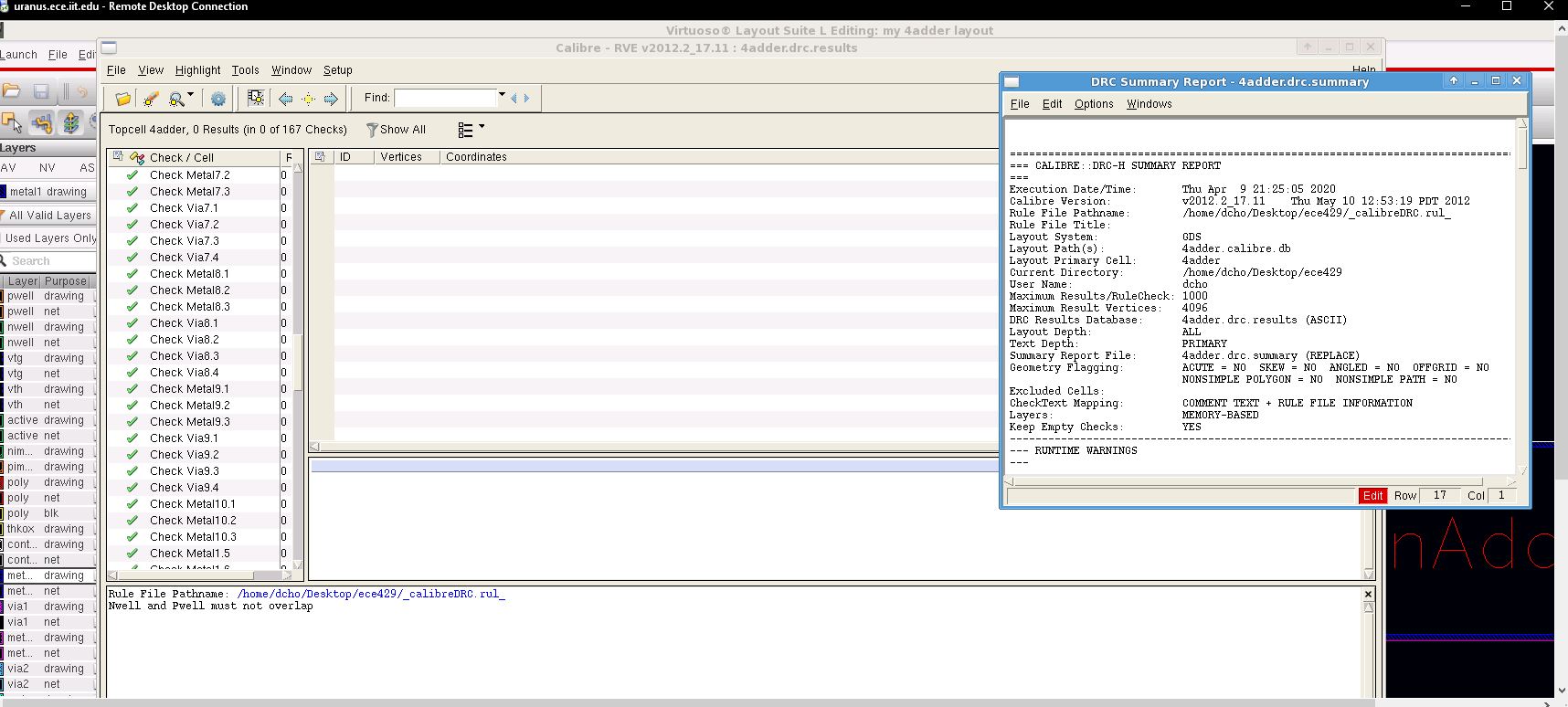
**Figure 4: 4-bit Adder Symbol**

****

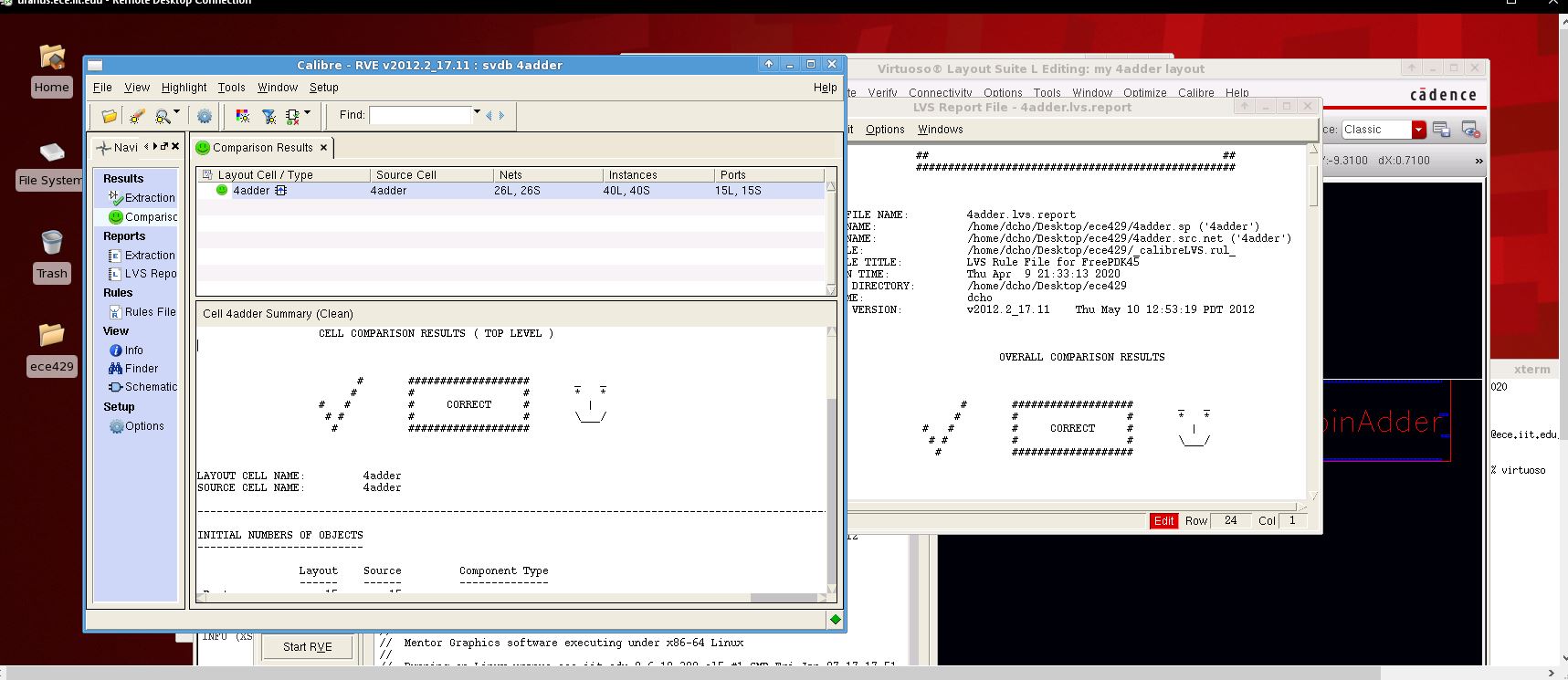
**Figure 5: 4-bit Adder layout**

****

**Figure 6: Layout DRC**

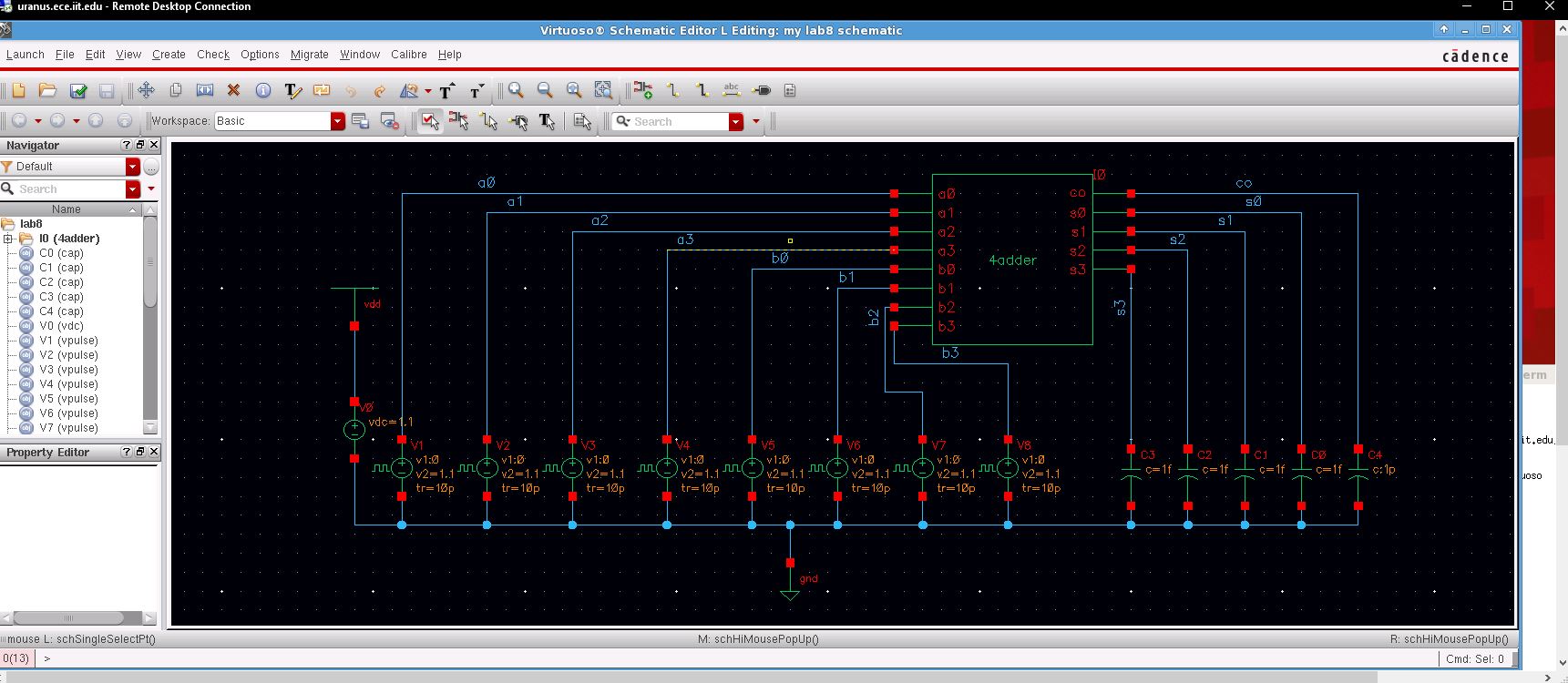
****

**Figure 7: Layout LVS**

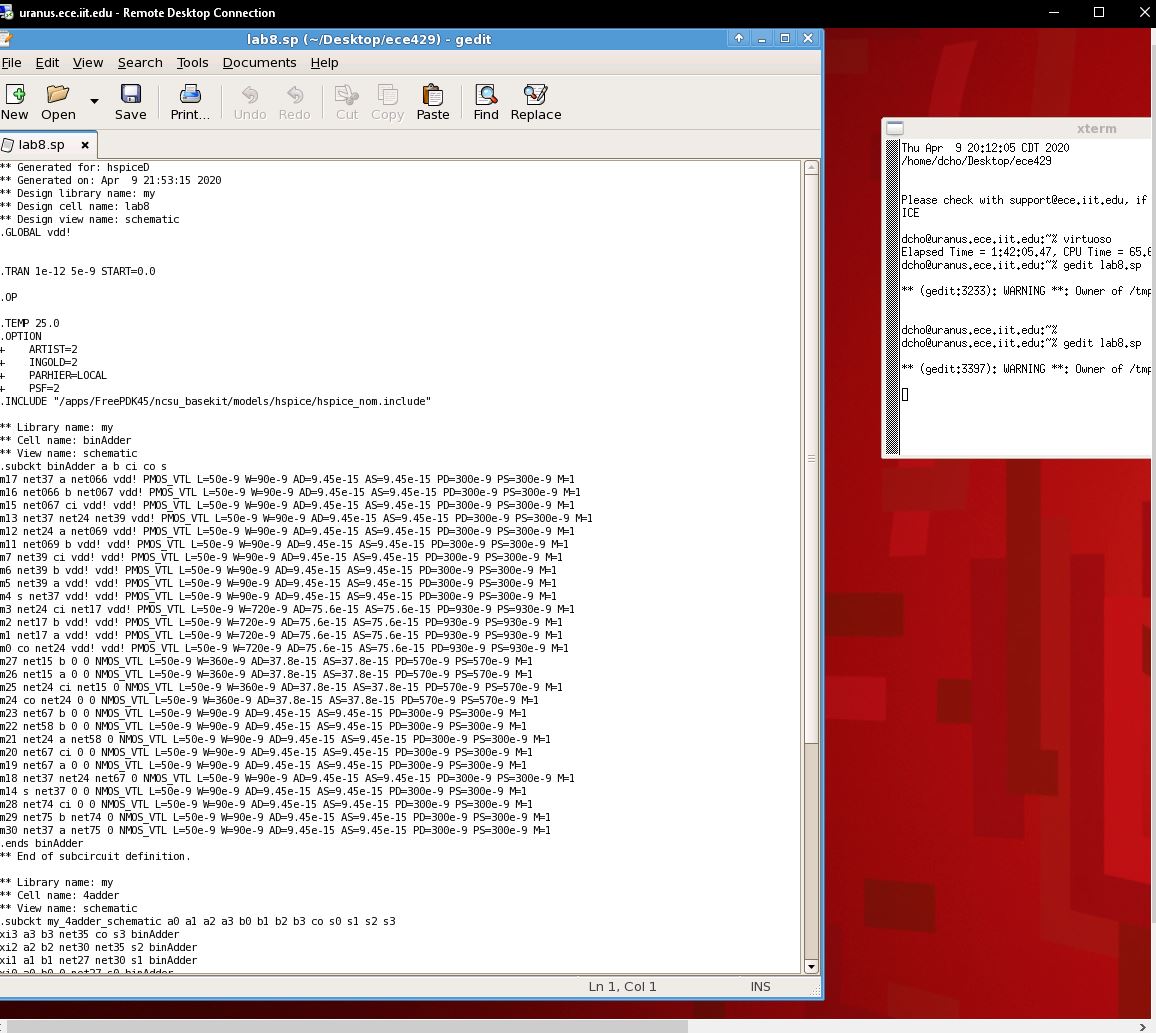
****

Afterwards, the test circuit was created using the previously created symbol. The test circuit was used to create a netlist for HSpice simulation. The netlist was edited to measure the delay when the inputs changed from 11 + 5 🡪 4 + 10.

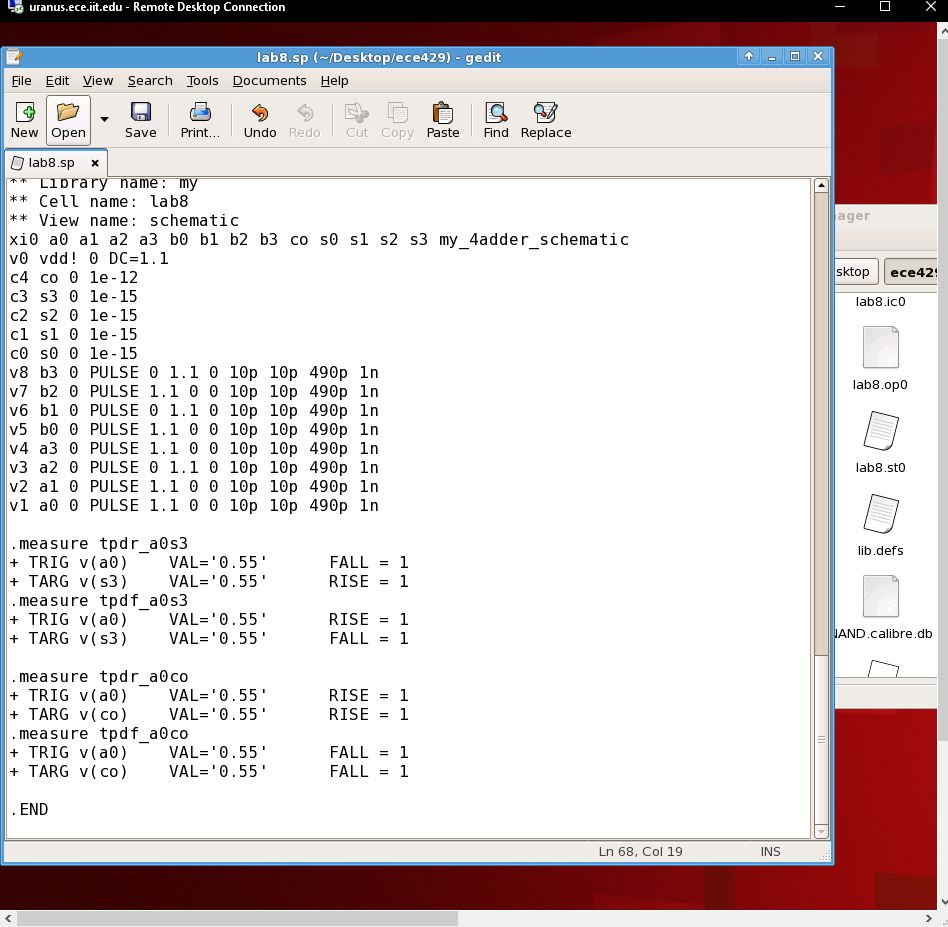
**Figure 8: Test Circuit**

****

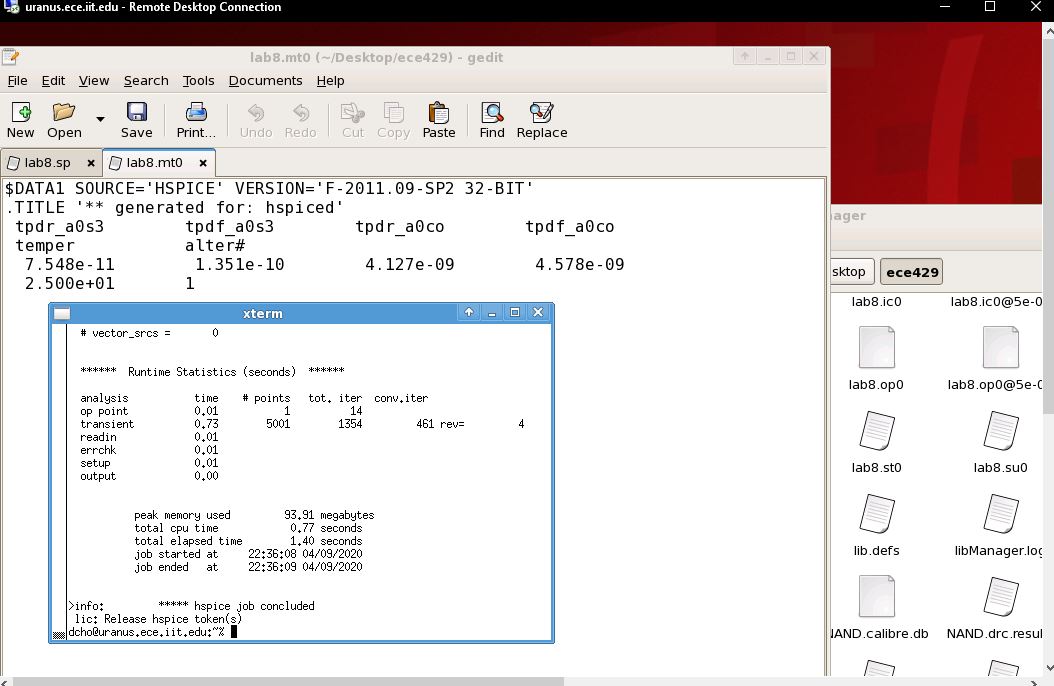
**Figure 9: Test Circuit Netlist**

****

**Figure 10: Modified Netlist**

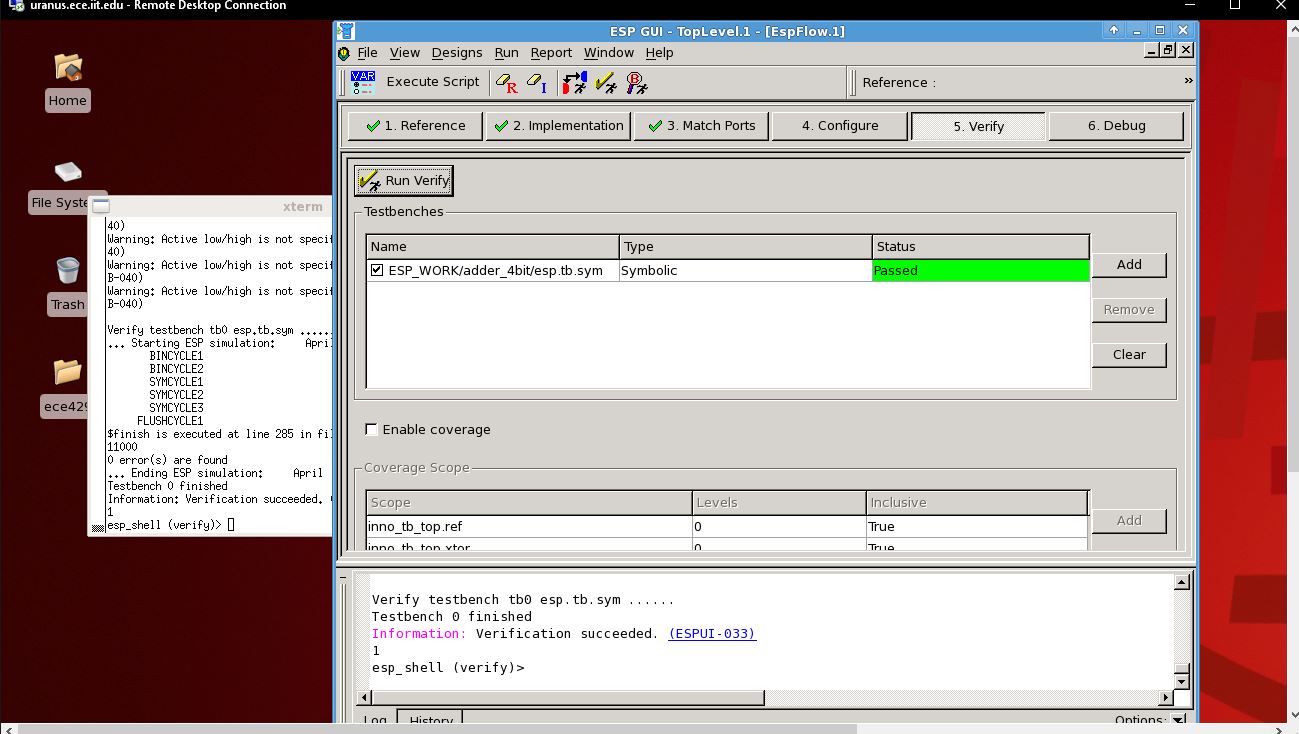
****

**Figure 11: Measurement File**

****

To finish, the layout was verified using the ESP GUI.

**Figure 12: ESP Pass**

****

**Conclusion**

In conclusion, this was a successful lab. Everything mostly went as expected, and all of the verifications were passed. The only issue is that the a0-co tpdr measurement did not have the expected.